



IRF630 IRF630FP

N-channel 200V - 0.35Ω - 9A TO-220/TO-220FP
Mesh overlay II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
IRF630	200V	<0.40Ω	9A
IRF630FP	200V	<0.40Ω	9A

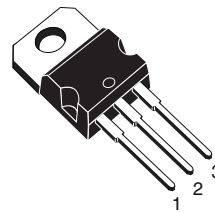
- Extremely high dv/dt capability
- Very low intrinsic capacitances
- Gate charge minimized

Description

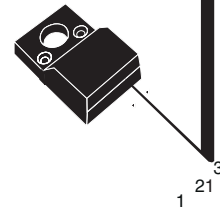
This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY process. This technology matches and improves the performances compared with standard parts from various sources.

Applications

- Switching application



TO-220



TO-220FP

Internal schematic diagram

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V _{DS}	Drain-source voltage (V _{GS} = 0)	200		V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 kΩ)	200		V
V _{GS}	Gate-source voltage	20		V
I _D	Drain current (continuous) at T _C = 25°C	9	9 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C =100°C	5.7	5.7 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	36	36 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25°C	75	30	W
	Derating factor	0.6	0.24	W/°C
dv/dt ⁽³⁾	Peak diode recover voltage slope	5		V/ns
V _{ISO}	Insulation withstand voltage (DC)	--	2000	V
T _J	Operating junction temperature	-65 to 150		°C
T _{stg}	Storage temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. ISD ≤ 9A, di/dt ≤ 300A/μs, VDD ≤ V(BR)DSS, Tj ≤ TJMAX

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
R _{thj-case}	Thermal resistance junction-case Max	1.67	4.17	°C/W
R _{thj-a}	Thermal resistance junction-ambient Max	62.5		°C/W
R _{thc-sink}	Thermal resistance case-sink typical	0.5		°C/W
T _l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	9	A
E _{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	160	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate bod leakage current ($V_{DS} = 0$)	$V_{GS} = . 20V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 4.5A$		0.35	0.40	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 4.5A$	3	4		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		540 90 35	700 120 50	pF pF pF
$t_{d(on)}$ t_r	Turn-on Dela Time Rise Time	$V_{DD} = 100V, I_D = 4.5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 14)		10 15	14 20	ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 160V, I_D = 9A$ $V_{GS} = 10V$		31 7.5 9	45	nC nC nC

1. Pulsed: pulse duration=300 μs , dut c cle 1.5%

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=9A, V_{GS}=0$			1.5	V
t_{rr}	Reverse recover time	$I_{SD}=9A,$ $di/dt = 100A/\mu s,$ $V_{DD}=50V, T_j=150^{\circ}C$ (see Figure 16)		170		ns
Q_{rr}	Reverse recover charge			0.95		nC
I_{RRM}	Reverse recover current			11		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

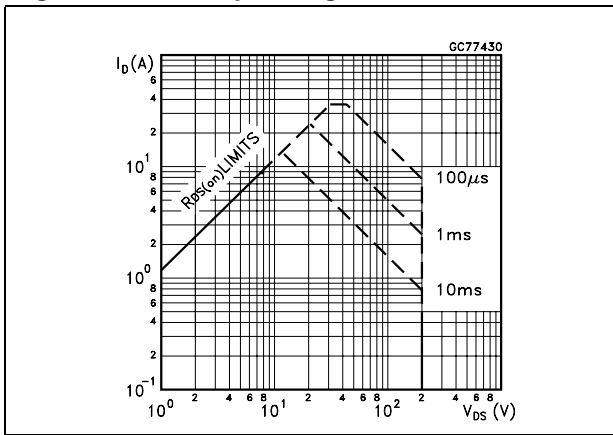


Figure 2. Thermal impedance for TO-220

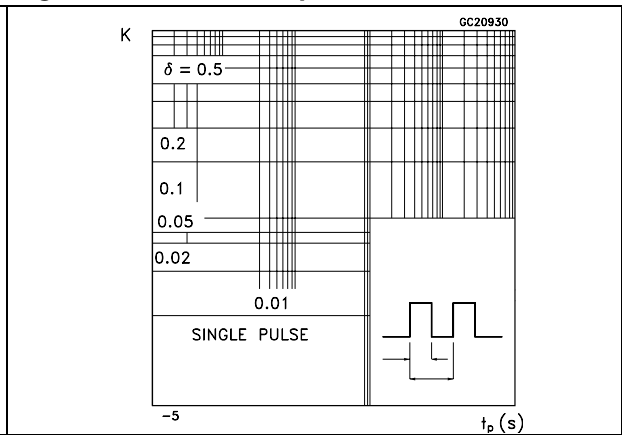


Figure 3. Safe operating area for TO-220/FP



Figure 4. Thermal impedance for TO-220/FP

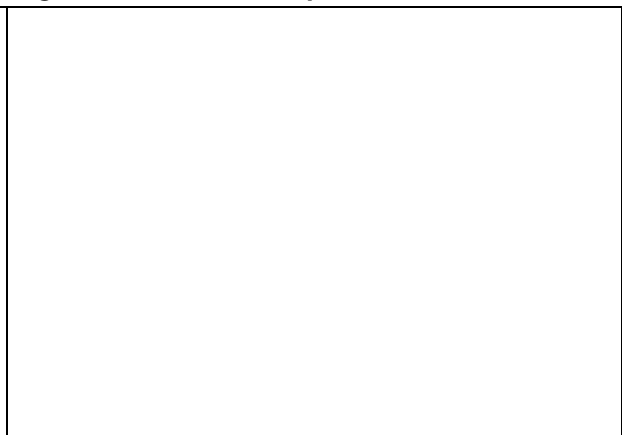


Figure 5. Output characteristics



Figure 6. Transfer characteristics



Figure 7. Transconductance

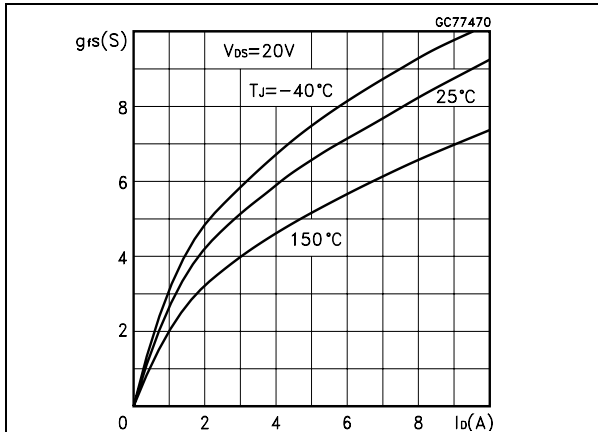


Figure 8. Static drain-source on resistance

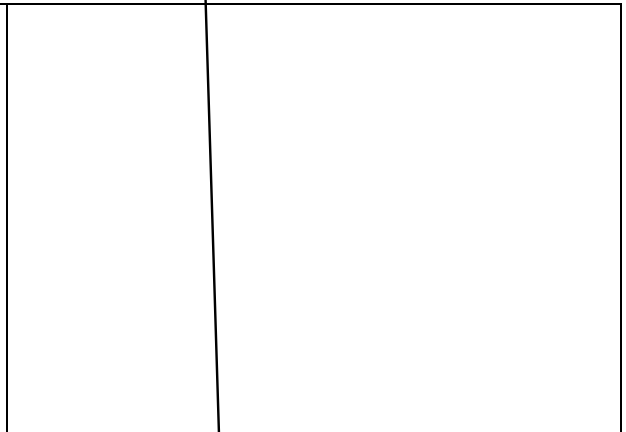
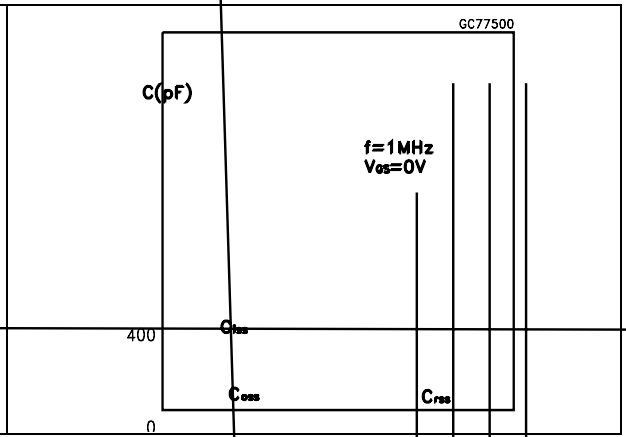
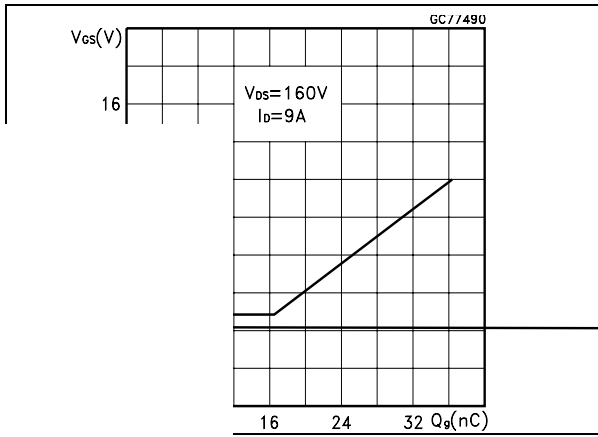


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations



Normalized gate threshold voltage vs temperature

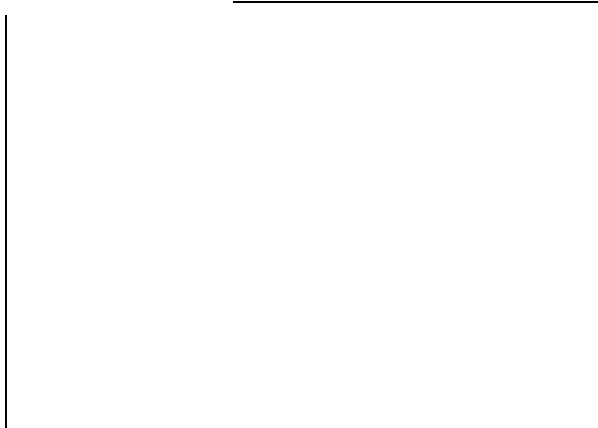


Figure 12. Normalized on resistance vs temperature

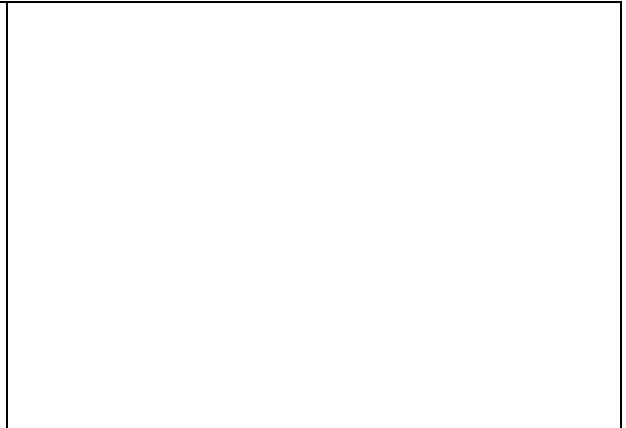
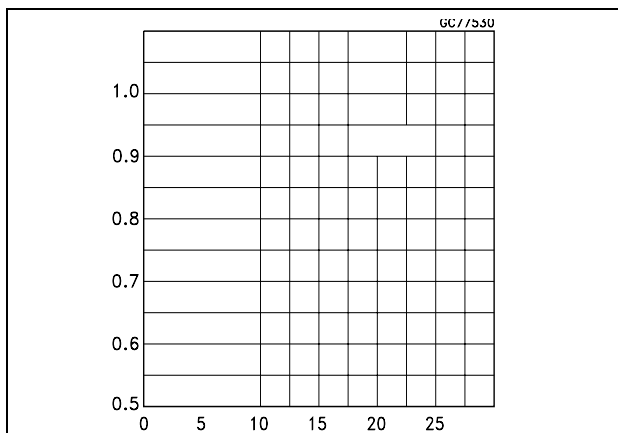


Figure 13. Source-drain diode forward characteristics



3 Test circuit

Figure 14. Switching times test circuit for resistive load

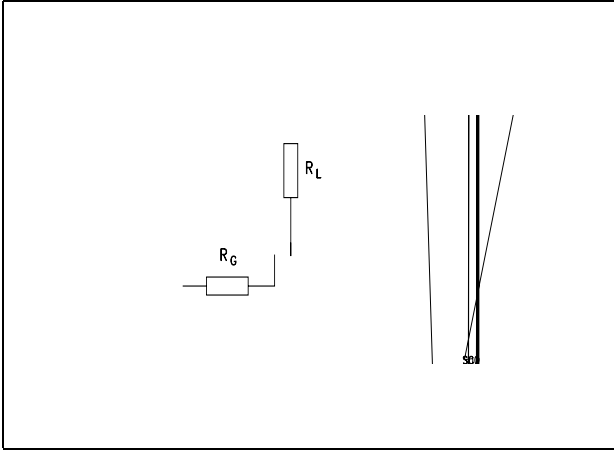
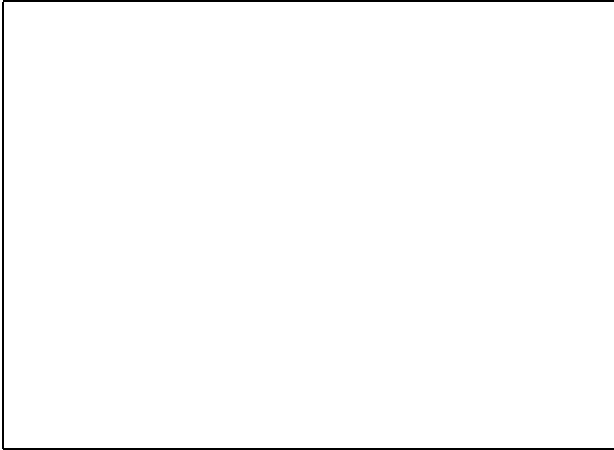


Figure 15. Gate charge test circuit



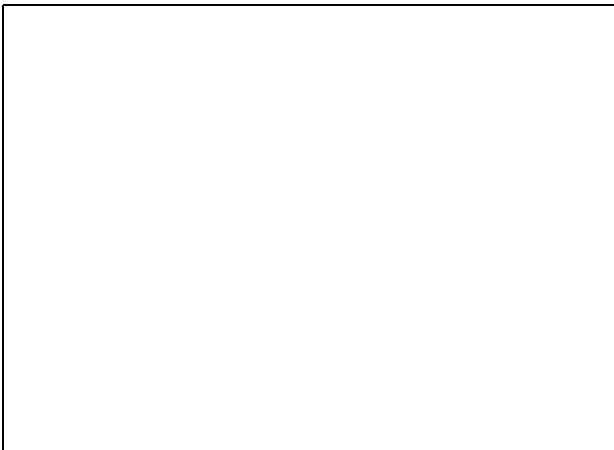
Figure 16. Test circuit for inductive load switching and diode recovery times



Figure



Figure 18. Unclamped inductive waveform



Figure

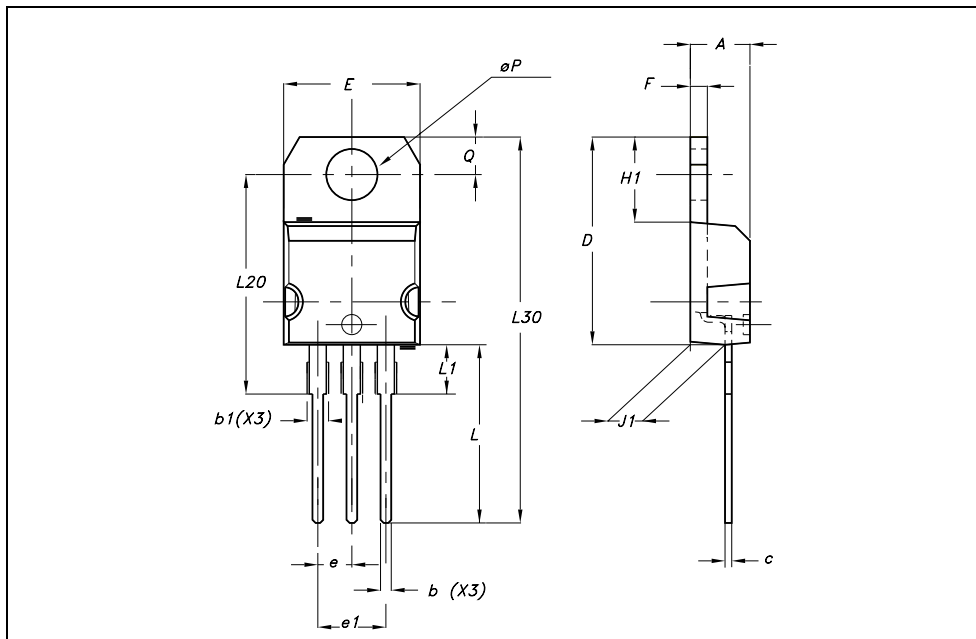


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

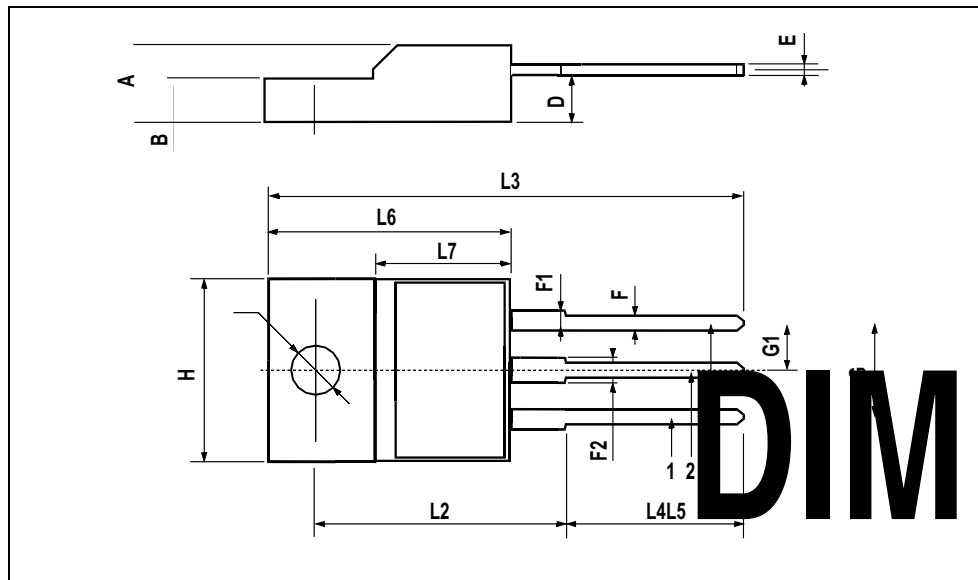
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



3

F2



5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	8	Complete version
03-Aug-2006	9	New template, no content change

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