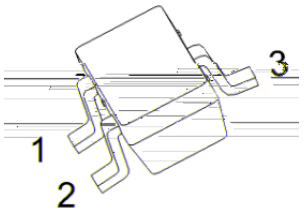
JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD

SOT-23-3L Plastic-Encapsulate MOSFETS

CJK3401AH P-Channel Enhancement Mode Field Effect Transistor

$V_{(BR)DSS}$	$R_{DS(on)}$MAX	I_D
-30V	50 mΩ@-10V	-4.2A
	60 mΩ@-4.5V	
	85 mΩ@-2.5V	

SOT-23-3L



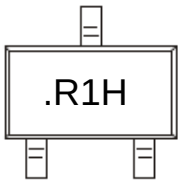
FEATURE

- High dense cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATION

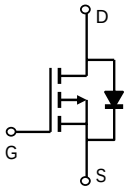
- Load Switch for Portable Devices
- DC/DC Converter

MARKING



Solid dot = Green molding compound device, if none,the normal device.

Equivalent Circuit



Maximum ratings (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	-4.2	A
Drain Current-Pulsed (not 1)	I_{DM}	-27	A
Power Dissipation	P_D	450	
Thermal Resistance from Junction to Ambient (t<5s)	$R_{\theta JA}$	313	℃
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~+150	℃

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-30			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-24V,V_{GS} = 0V			-1	μA
Gate-source leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V			±100	nA
On characteristics						
Drain-source on-resistance (note 1)	$R_{DS(on)}$	V_{GS} =-10V, I_D =-4A			50	mΩ
		V_{GS}=-4.5V, I_D =-3.5A		47	60	mΩ
		V				

SOT-23-3L Package Outline Dimensions

SOT-23-3L Suggested Pad Layout

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad la

SOT-23-3L Embossed Carrier Tape

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